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10/028,298	12/19/2001	David N. Goldberg	10019867-1	2928
7590	08/08/2007		EXAMINER	
HEWLETT-PACKARD COMPANY Intellectual Property Administration P.O. Box 272400 Fort Collins, CO 80527-2400			HO, CHUONG T	
			ART UNIT	PAPER NUMBER
			2616	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/028,298	GOLDBERG ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	CHUONG T. HO	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 11 May 2007.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,3-9,11-17,19-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1,3-9,11-17,19-24 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

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1. The amendment filed 05/11/07 have been entered and made of record.

***Response to Arguments***

2. Applicant's arguments filed 05/11/07 have been fully considered but they are not persuasive.

In the page 6, lines 5-8, the applicant alleged that "Claims 1, 3-9, 11-17 and 19-24 are rejected under 35 U.S.C 103 (a) as being obvious over U.S.Patent Publication 2003/0101367 by Bartfai et al. (referred to hereinafter as "Barfai") in view of U.S.Patent 6,654,908 by Lindsy et al. (referred to hereinafter as "Lindsay")"

The examiner respectfully disagrees.

In reviewing Non final action mail 02/06/07, claims 1, 9, 17 are rejected under 35 U.S.C. 103(a) as being obvious over Bartfai et al. (U.S.Patent No. 2003/0101367 A1) in view of Owen et al. (U.S.Patent No. 6,760,838 B2), Not Claims 1, 9, 17 are rejected under 35 U.S.C 103 (a) as being obvious over U.S.Patent Publication 2003/0101367 by Bartfai et al. (referred to hereinafter as "Barfai") in view of U.S.Patent 6,654,908 by Lindsy et al. (referred to hereinafter as "Lindsay")

Therefore, the Applicant's argument is not persuasive.

In the page 7, lines 20-24, the applicant alleged that "Neither Bartfail nor Lindsay teach or suggest, " setting a link usage indicator in a first storage element by reach of said communicating nodes prior to communication therebetween, and wherein each of said communication nodes has a corresponding position in said first storage element".

The examiner respectfully disagrees.

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Bartfai et al. (U.S.Patent No. 2003/0101367 A1) discloses setting a link usage indicator (page 2, [0007], error condition) in a first storage element (page 2, [0007], error registers) by reach of said communication nodes prior to communication therebetween, and wherein each of said communication nodes has a corresponding position (page 2, [0007], position) in said first storage element (page 2, [0007], The error handling method comprises the steps of detecting an error condition in an affected adapter connected to one of the nodes. The nature of the error is indicated by specific bit positions in error registers within the affected adapter. In the present invention some of these bits provide an error condition indicator which signals that recovery is possible but may take longer than the usually allotted time for recovery).

Owen et al. (U.S.Patent No. 6,760,838 B2) discloses setting a link usage indicator (col. 12, lines 55-67, link failure bit indicates) in a first storage element (col. 12, lines 55-67, link control register 98) by reach of said communicating nodes prior to communication therebetween, and wherein each of said communication nodes has a corresponding position (col. 2, lines 54-56, col. 3, lines 34-36, location) in said first storage element.

3. Claims 1, 3-8, 9, 11-16, 17, 19-24 are pending.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

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Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 9, 17 are rejected under 35 U.S.C. 103(a) as being obvious over Bartfai et al. (U.S. Patent No. 2003/0101367 A1) in view of Owen et al. (U.S. Patent No. 6,760,838 B2).

In the claim 1, Bartfai discloses a method of error protection comprising: detecting an error during communication between nodes in a network, said nodes separated by a link; blocking (see page 3, [0028], page 5, [0046], claim 1) further communication between said nodes in response to said detected error; unblocking (see page 3, [0029], page 6, [0046], claim 1) said blocked communication between said nodes, provided said communicating nodes have resolved said detected error, wherein said communication between said nodes is re-enabled; setting a link usage indicator in a first storage (register) by each of said communicating nodes prior to communication there between (resetting by the adapter, see col. 2, lines 5-10, the nature of the error is indicated by specific bit position in error registers within the affected adapter) (see col. 3, lines 5-10, problem clearance is indicated when restarted completes successfully as indicated by the contents of interrupt vector registers.....Once the relevant interrupt vector register bits are reset or are no longer indicate an active error severity status).

However, Bartfai is silent to disclosing wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element.

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Owen et al. disclose setting (see figure 7, col. 12, lines 55-67, bit 3, CRC Error, checking a status register, Bit 0 = 1: link OK; Bit 0 = 0: link Not OK) a link usage indicator in a first storage element by each of communicating nodes prior to communication therebetween, and wherein each of said communicating nodes (figure 7, col. 20, lines 18-20, node ID in the register) has a corresponding position in said first storage element, and wherein said link usage indicator set (figure 6, figure 7, figure 11A) by each of said nodes is relative to said corresponding position in said first storage element (see col. 12, lines 30-35 the command register of the capability block 90 for the interface, col. 12, lines 40-45, the bits in the command register are writable by software, with the execution of the unit count field and the master host unit which automatically set).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Bartfai with the teaching of Owen to provide wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

6. In the claim 9, Bartfai discloses a method of error protection comprising: detecting an error during communication between nodes in a network, said nodes separated by a link; blocking (see page 3, [0028], page 5, [0046], claim 1) further

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communication between said nodes in response to said detected error; unblocking (see page 3, [0029], page 6, [0046], claim 1) said blocked communication between said nodes, provided said communicating nodes have resolved said detected error, wherein said communication between said nodes is re-enabled; setting a link usage indicator in a first storage (register) by reach of said communicating nodes prior to communication there between (resetting by the adapter, see col. 2, lines 5-10, the nature of the error is indicated by specific bit position in error registers within the affected adapter) (see col. 3, lines 5-10, problem clearance is indicated when restarted completes successfully as indicated by the contents of interrupt vector registers.....Once the relevant interrupt vector register bits are reset or are no longer indicate an active error severity status).

However, Bartfai is silent to disclosing wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element.

Owen et al. disclose setting (see figure 7, col. 12, lines 55-67, bit 3, CRC Error, checking a status register, Bit 0 = 1: link OK; Bit 0 = 0: link Not OK) a link usage indicator in a first storage element by reach of communicating nodes prior to communication therebetween, and wherein each of said communicating nodes (figure 7, col. 20, lines 18-20, node ID in the register) has a corresponding position in said first storage element, and wherein said link usage indicator set (figure 6, figure 7, figure 11A) by each of said nodes is relative to said corresponding position in said first storage element (see col. 12, lines 30-35 the command register of the capability block 90 for the

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interface , col. 12, lines 40-45, the bits in the command register are writable by software, with the execution of the unit count field and the master host unit which automatically set).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Bartfai with the teaching of Owen to provide wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

7. In the claim 17, Bartfai discloses a communication interconnect (figure 1); an optional display device coupled to said communication interconnect (it is inherent that an optional display device is connected to at least one node in order to monitor and execute software programs and application (paragraphs [0002] [0003])); and a processor coupled to said communication interconnected (paragraph [0003]); blocking (see page 3, [0028], page 5, [0046], claim 1) further communication between said nodes in response to said detected error; unblocking (see page 3, [0029], page 6, [0046], claim 1) said blocked communication between said nodes, provided said communicating nodes have resolved said detected error, wherein said communication between said nodes is re-enabled; setting a link usage indicator in a first storage (register) by each of said communicating nodes prior to communication there between (resetting by the

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adapter, see col. 2, lines 5-10, the nature of the error is indicated by specific bit position in error registers within the affected adapter) (see col. 3, lines 5-10, problem clearance is indicated when restarted completes successfully as indicated by the contents of interrupt vector registers....Once the relevant interrupt vector register bits are reset or are no longer indicate an active error severity status).

However, Bartfai is silent to disclosing wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element.

Owen et al. disclose setting (see figure 7, col. 12, lines 55-67, bit 3, CRC Error, checking a status register, Bit 0 = 1: link OK; Bit 0 = 0: link Not OK) a link usage indicator in a first storage element by each of communicating nodes prior to communication therebetween, and wherein each of said communicating nodes (figure 7, col. 20, lines 18-20, node ID in the register) has a corresponding position in said first storage element, and wherein said link usage indicator set (figure 6, figure 7, figure 11A) by each of said nodes is relative to said corresponding position in said first storage element (see col. 12, lines 30-35 the command register of the capability block 90 for the interface, col. 12, lines 40-45, the bits in the command register are writable by software, with the execution of the unit count field and the master host unit which automatically set).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Bartfai with the teaching of Owen to provide

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wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 3-8, 11-16, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over combined system (Bartfai – Owen) in view of Lindsay (U.S.Patent No. 6,654,908 B1).

In the claim 3, Bartfai et al. disclose the limitations of claim 1 above.

However, the combined system (Bartfai – Owen) are silent to disclosing wherein said detection of said error causes a generation of an error indicator, said error indicator stored in a second storage element.

Lindsay discloses wherein said detection of said error causes a generation of an error indicator, said error indicator stored in a second storage element (figure 2, col. 6,

lines 27-30, if the status register is set to indicate an error, the compute element reads the tag register for the specific error type).

Both Bartfai, Owen, and Lindsay disclose error detection. Lindsay recognizes wherein said detection of said error causes a generation of an error indicator, said error indicator stored in a second storage element. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Bartfai – Owen) with the teaching of Lindsay to detect of said error causes a generation of an error indicator, said error indicator stored in a second storage element in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

10. In the claim 4, Bartfai discloses the limitations of claim 1 above.

However, the combined system (Bartfai – Owen) is silent to disclosing activating a blocking agent to provide said blocking of said communication, said blocking agent activated in response to said generation of said error indicator. Lindsay discloses activating a blocking agent to provide said blocking of said communication, said blocking agent activated in response to said generation of said error indicator (see figure 2, col. 6, lines 27-30).

Both Bartfai, Owen, and Lindsay disclose error detection. Lindsay recognizes activating a blocking agent to provide said blocking of said communication, said blocking agent activated in response to said generation of said error indicator. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to

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modify the combined system (Bartfai – Owen) with the teaching of Lindsay to activate a blocking agent to provide said blocking of said communication, said blocking agent activated in response to said generation of said error indicator in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

11. In the claim 5, Bartfai discloses resolving of said detected error is performed by each of said communicating nodes, and is in a manner appropriate for each node (see paragraph 29 , 30).

12. In the claim 6, Bartfai discloses the limitations of claim 1 above.

However, the combined system (Bartfai – Owen) are silent to disclosing generating multiple clearing by said nodes, wherein each of said nodes generating one of said multiple clearing indicators subsequent to it said resolving of said error, wherein each of said clearing indicators corresponds to an associated corresponding position relative to said nodes, and wherein each of said clearing indicators resets a link usage indicators set by each of said nodes.

Lindsay discloses generating multiple clearing indicators (see col. 4, lines 20-22) by said nodes, wherein each of said nodes generating one of said multiple clearing indicators subsequent to it said resolving of said error, wherein each of said clearing indicators corresponds to an associated corresponding position relative to said nodes, and wherein each of said clearing indicators resets (see col. 3, lines 65-67) a link usage indicators set by each of said nodes.

Both Bartfai, Owen, and Lindsay disclose error detection. Lindsay recognizes generating multiple clearing by said nodes, wherein each of said nodes generating one of said multiple clearing indicators subsequent to it said resolving of said error, wherein each of said clearing indicators corresponds to an associated corresponding position relative to said nodes, and wherein each of said clearing indicators resets a link usage indicators set by each of said nodes . Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Bartfai – Owen) with the teaching of Lindsay to generate multiple clearing by said nodes, wherein each of said nodes generating one of said multiple clearing indicators subsequent to it said resolving of said error, wherein each of said clearing indicators corresponds to an associated corresponding position relative to said nodes, and wherein each of said clearing indicators resets a link usage indicators set by each of said nodes in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

13. In the claim 7, Bartfai discloses a first storage element and second storage element are disposed in said link (figure 2, reference 162, paragraph [0003]. Memory in adapter is interpreted as storage element and is disposed in a link connected to the adapter.

14. In the claim 8, Bartfai discloses a first storage element and second storage element are disposed in each said node (paragraph [0004]); memory in a node is interpreted as storage element disposed in each node.

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15. In the claim 11, claim 11 is rejected the same reason of claim 3 above.
16. In the claim 12, claim 12 is rejected the same reason of claim 4 above.
17. In the claim 13, claim 13 is rejected the same reason of claim 5 above.
18. In the claim 14, claim 14 is rejected the same reason of claim 6 above.
19. In the claim 15, claim 15 is rejected the same reason of claim 7 above.
20. In the claim 16, claim 16 is rejected the same reason of claim 8 above.
21. In the claim 19, claim 19 is rejected the same reason of claim 3 above.
22. In the claim 20, claim 20 is rejected the same reason of claim 4 above.
23. In the claim 21, claim 21 is rejected the same reason of claim 5 above.
24. In the claim 22, claim 22 is rejected the same reason of claim 6 above.
25. In the claim 23, claim 23 is rejected the same reason of claim 7 above.

In the claim 24, claim 24 is rejected the same reason of claim 8 above. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Conclusion***

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bartfai et al. (U.S. Patent No. 7,093,154 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571) 272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ORGAD EDAN can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

08/05/08

EDAN ORGAD  
PRIMARY PATENT EXAMINER

*Edan Orgad 8/6/08*